An important relation between threshold voltage and the density of interfacial defect states in Poly-Si TFTs

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Abstract
Interface defect states of polycrystalline silicon thin-film transistors (poly-Si TFTs) play important role in the degradation of subthreshold characteristics. In this paper, an investigation of interface states is taken on, results show that both the threshold voltage and the difference between the threshold voltage and the gate voltage corresponding to the minimum drain current are proportional to the density of interface states at the SiO$_2$/poly-Si interface, and results fit well with the experimental data.

Keywords: poly-Si, thin film transistor, interface defect states

1. Introduction
With the development of research and fabrication process in thin-film transistors (TFTs), applications of polycrystalline silicon (poly-Si) TFTs gradually tend to be popularized, such as active matrix liquid-crystal displays (AMLCD) [1, 2] and organic light-emitting diode (OLED)[3]. Contrast with the amorphous silicon, the poly-Si shows higher mobility. However,
one major limitation as related to poly-Si is defect states. Most models of poly-Si TFT [4-10] pay more attentions to bulk defects, but few focus on interface states. What’s more, along with the decreasing of the grain size [11], the influence of defect states at the interface on the TFT’s performance became more evident in comparison with that in poly-Si. Therefore, theoretical investigations on interface states can represent a useful tool to improve the performance of TFTs based on poly-Si.

As to n type poly-Si TFT, when the positive gate voltage $V_{gs}$ is smaller than the threshold voltage ($V_{th}$), that is to say, $V_o<V_{gs}<V_{th}$, where $V_o$ is the gate voltage corresponding to the minimum drain current, the TFT is working in the subthreshold regime [9]. If the operation range of subthreshold region can be reduced, the switching characteristic would be greatly improved.

In this paper, we describe briefly the effect of interface states on the device performance, the calculation and the modeling are presented in second section. Finally, the main conclusions are given in the last part.

2. Model development

1. Relation of $V_{th}$-$V_o$ and the density of interface defect states

Due to the defect states, the transfer characteristic curve of the poly-Si TFT is more gently than that of the MOSFET[9]. The Fig 1 presents the transfer characteristic curve of the poly-Si TFT

![Fig.1 transfer characteristic curve of the poly-Si TFT](image)
Based on homothetic triangle theory,

\[
\frac{V_{g,max} - V_o}{V_{th} - V_o} = \frac{I_{ds1}}{I_{ds2}}
\]

(1)

where \(V_{g,max}\) is the gate voltage corresponding to the maximum transconductance of the poly-Si TFT, \(I_{ds1} , I_{ds2}\) are drain current corresponding to the \(V_{g,max}\) and the \(V_{th}\), respectively.

From Eq.(1), the following can be obtained:

\[
\frac{V_{g,max} - V_{th}}{V_{th} - V_o} = \frac{I_{ds1} - I_{ds2}}{I_{ds2}}
\]

(2)

As the subthreshold swing satisfies[1]:

\[
S = \frac{dV_{gs}}{d \log I_{ds}} = 2.3 \frac{I_{ds}dV_{gs}}{dI_{ds}} = C + DN_t
\]

(3)

where \(C\) and \(D\) are constants; \(N_t\) is the density of defect states at the SiO\(_2\)/poly-Si interface.

After some algebraic manipulation, Eq. (3) can be rewritten as:

\[
dI_{ds} = \frac{2.3I_{ds}dV_{gs}}{C + DN_t}
\]

(4)

Theoretically, the curve can be almost a straight line if the angle is small enough. Therefore, one can get

\[
dI_{ds} = I_{ds1} - I_{ds2}
\]

(5)

\[
dV_{gs} = V_{g,max} - V_{th}
\]

(6)

Substitute Eqs.(5)(6) into Eq.(2), then:

\[
V_{th} - V_o = E + FN_t
\]

(7)

where \(E\) and \(F\) are constants.

II. Relation of \(V_{th}\) and the density of interface defect states

Assume the defect states are distributed at the interface only, then the current of the poly-Si TFT can be given by[10]:

\[
\frac{\Delta I_{ds}}{I_{ds,lin}} = KN_t
\]

(8)

where \(K\) is a constant, \(\gamma\) is a fitting factor related to the short channel effect and \(I_{ds,lin}\) is the
drain current in the subthreshold regime.

As the drain voltage is small, the drain current can be expressed as[12]:

\[ I_{ds} = \frac{W}{L} \mu_{\text{eff}} C_{ox} (V_{gs} - V_{th} - \frac{V_{ds}}{2})V_{ds} \]  \hspace{1cm} (9)

\( \mu_{\text{eff}} \) is the effective mobility. Combining Eq.(8) with Eq.(9):

\[ V_{th} \propto N_{i} \]  \hspace{1cm} (10)

3. Results and discussion

Two-dimensional device simulations are effective for investigating the underlying physics of device operation. In this section, we used the device simulator MEDICI for modeling. The device parameters used in simulation are listed in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>doping concentration of the source and drain</td>
<td>(1 \times 10^{22}) cm(^{-3})eV(^{-1})</td>
</tr>
<tr>
<td>doping concentration of the channel</td>
<td>(1 \times 10^{16}) cm(^{-3})eV(^{-1})</td>
</tr>
<tr>
<td>poly-Si layer thickness</td>
<td>100nm</td>
</tr>
<tr>
<td>Insulator thickness</td>
<td>30nm</td>
</tr>
<tr>
<td>TFT flat-band voltage</td>
<td>0.7V</td>
</tr>
<tr>
<td>Channel length</td>
<td>2.5(\mu)m</td>
</tr>
<tr>
<td>Channel width</td>
<td>80(\mu)m</td>
</tr>
</tbody>
</table>

With the consideration of the lateral electric field[13], simulation results are presented in Fig 2, Fig 3 and Fig 4. Fig. 4 shows the comparison of experimental results[14] with modeling results of relation of threshold voltage and interfacial state densities.
Fig. 2: relation of subthreshold swing with the interface states

Fig. 3: relation of $V_{th}-V_{a}$ and the density of interface defect states
Combining Eqs.(7)(10) with simulation results, we can have a conclusion that the difference between the threshold voltage and the gate voltage corresponding to the minimum drain current \((V_{th}-V_o)\) is proportional to the density of interface defect states, which means the operation range of subthreshold region is linearly with the density of interface states. Besides, the threshold voltage \((V_{th})\) shows linear relationship with the density of interface states as well, which is in conformity with the Redinger’s assumption [15].

### 4. Conclusion

With the development of poly-Si TFTs, understanding the influence of interface defect states may be helpful in providing insight into routes to reduce this undesired effect. In this paper, an investigation of interface defect states is presented, results show that both the difference between the threshold voltage and the gate voltage corresponding to the minimum drain current and the threshold voltage are proportional to the density of interface states, results fit well with the experimental data.

### 5. Acknowledge

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References


