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A new extraction method of threshold voltage based on temperature effect of a-Si:H TFT

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Abstract

Based on the double exponential distributions of trap states in the channel of the hydrogenated amorphous silicon thin film transistor (a-Si:H TFT), a new extraction method of the threshold voltage for a-Si:H TFTs has been developed. By taking advantage of the conductivity, the expression of the drain current corresponding to the threshold voltage is obtained. The inclusion of the temperature effect in our model makes accurate the extraction under different temperatures, and results fit well with the experimental data.

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***Keywords*:** amorphous, thin film transistor, threshold voltage, temperature

1. Introduction

Hydrogenated amorphous silicon [1] thin film transistors (a-Si:H TFTs) are widely used for

active matrix liquid-crystal displays (AMLCD) as they can be built on the large flexible or glass substrate at low cost [2, 3].

In the current situation, the threshold voltage is frequently extracted by the linear-extrapolation techniques, which are based on the assumption that the inversion charge increases linearly with the gate voltage above the threshold [4]. Although many models contain the temperature effect and the extraction of the threshold voltage [5-19], it is rare to put them together, including the AIM-SPICE level 15 model [20]. Moreover, in AMLCD drive circuits, the operation temperature of a-Si:H TFTs can reach to 70˚C [21]. Therefore, the temperature is an essential factor affecting the electrical properties and it is of importance to develop simple extraction methods that convenient for modeling with the consideration of the temperature effect.

In this paper, according to the conduction mechanisms that exist in a-Si:H TFTs at medium and high temperatures[14, 22-24], a new extraction method of the threshold voltage is proposed, in which the threshold voltage is defined as the gate voltage when the electron Fermi level moves into tail states [25]. One of the most important aspects that make the extraction method accurate is its consideration of the temperature and the defect states.

2. Model development

The densities of tail states n_t and deep states n_d in the channel can be expressed as [26]:

$$n_d = g_d \exp\left(\frac{E - E_C}{k_B T_d}\right) \tag{1}$$

$$n_t = g_t \exp\left(\frac{E - E_C}{k_B T_t}\right) \tag{2}$$

where k_B is the Boltzmann's constant, g_t and g_d are densities of tail states and deep states at the conduction band energy E_C, respectively. T_t and T_d are the characteristic temperatures in Kelvin.

The energy corresponding to the intersection of the two distributions can be gained by:

$$g_d \exp\left(\frac{E - E_C}{k_B T_d}\right) = g_t \exp\left(\frac{E - E_C}{k_B T_t}\right) \tag{3}$$

Eq.(3) yields

$$E - E_C = \frac{k_B T_t T_d}{T_d - T_t} \ln\left(\frac{g_d}{g_t}\right) \tag{4}$$

Define the threshold voltage as the gate voltage when the electron Fermi level moves from the deep states into tail states [26], that is:

$$E_{\mathrm{F}} - E_{\mathrm{C}} = \frac{k_{\mathrm{B}} T_{\mathrm{t}} T_{\mathrm{d}}}{T_{\mathrm{d}} - T_{\mathrm{t}}} \ln\left(\frac{\mathrm{g_d}}{\mathrm{g_t}}\right) \tag{5}$$

where E_{F} is the Fermi level. As the conductivity can be expressed as [12]:

$$\sigma = \sigma_0 \exp\left(\frac{E_{\mathrm{F}} - E_{\mathrm{C}}}{k_{\mathrm{B}} T}\right) \tag{6}$$

Substitute Eq(5) into Eq(6), one can obtain:

$$\sigma = \sigma_0 \left(\frac{\mathrm{g_d}}{\mathrm{g_t}}\right)^{\frac{T_{\mathrm{t}} T_{\mathrm{d}}}{T(T_{\mathrm{d}} - T_{\mathrm{t}})}} \tag{7}$$

where σ_0 is a constant that ranges from100S/cm to 200S/cm [27-30], then, the drain current corresponding to the threshold voltage can be given by:

$$I_{\mathrm{ds}} = \frac{W}{L} \int_0^{t_{\mathrm{Si}}} \int_0^{L} \left(\sigma \frac{\mathrm{d}V_{\mathrm{ch}}}{\mathrm{d}y}\right) \mathrm{d}x\mathrm{d}y = \frac{W}{L} t_{\mathrm{Si}} \int_0^{V_{\mathrm{ds}}} \sigma \mathrm{d}V_{\mathrm{ch}} = \frac{W}{L} t_{\mathrm{Si}} \int_0^{V_{\mathrm{ds}}} \sigma_0 \left(\frac{\mathrm{g_t}}{\mathrm{g_d}}\right)^{\frac{T_{\mathrm{t}} T_{\mathrm{d}}}{T(T_{\mathrm{t}} - T_{\mathrm{d}})}} \mathrm{d}V_{\mathrm{ch}} = \frac{W}{L} t_{\mathrm{Si}} V_{\mathrm{ds}} \sigma_0 \left(\frac{\mathrm{g_t}}{\mathrm{g_d}}\right)^{\frac{T_{\mathrm{t}} T_{\mathrm{d}}}{T(T_{\mathrm{t}} - T_{\mathrm{d}})}} \tag{8}$$

Here, x and y are the position coordinates along the channel depth and the channel length direction, respectively. Consequently, under certain temperature and drain voltage, the threshold voltage can be defined as the gate voltage when the drain current is equal to the value of Eq(8).

3. Results and discussion

Two-dimensional device simulations are effective for investigating the underlying physics of device operation. In this section, we used the device simulator MEDICI for modeling. This DOS model applied in simulation is shown in Fig.1, which is put forward by Shur and Hack. Other device parameters used in simulation are listed in Table 1. Fig.2 presents the measured [26] and modeled output characteristic curves of the a-Si:H TFT. Fig.3 displays the transfer characteristic curves under different temperatures of the a-Si:H TFT. Fig. 4 shows the comparison of experimental results with modeling results [6], it is demonstrated that the model exhibits a reasonable agreement with the measured data and more accurate than the linear-extrapolation technique. Moreover, Fig. 4 indicates that the threshold voltage depends linearly on the operation temperature of the a-Si:H TFT [31] and V_{th} values are overestimated by using the linear extrapolation.

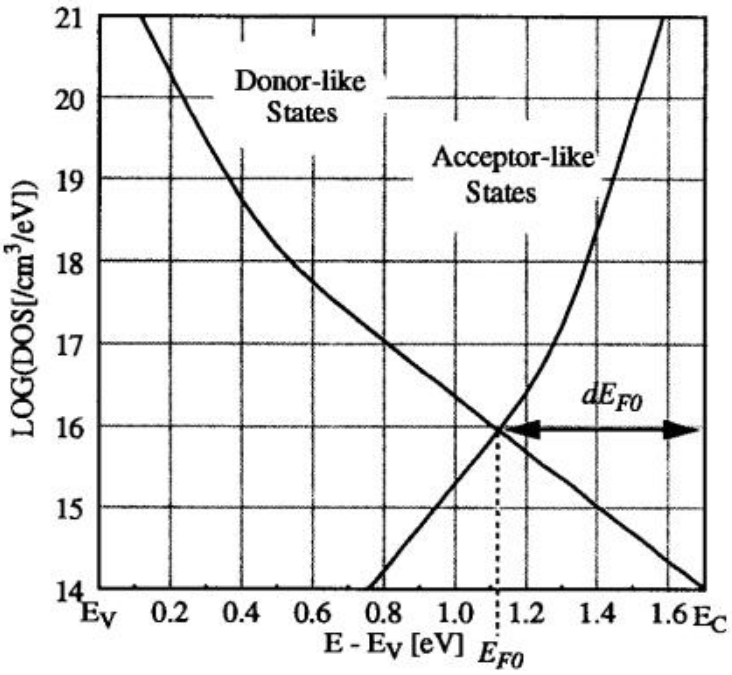

Fig.1 Distribution of trap states in the amorphous silicon bandgap.

Table 1 [26] Parameters used in 2-D simulations

Band gap of a-Si:H	E_g	1.72eV
Bulk Fermi level	E_{f0}	0.65eV
Effective density of states in the conduction band	N_C	7×10^{19}cm^{-3}
Deep states density at E_C	g_d	8.8×10^{18}cm^{-3}eV^{-1}
Tail states density at E_C	g_t	2.1×10^{22}cm^{-3}eV^{-1}
Deep states characteristic temperature	T_d	997K
Tail states characteristic temperature	T_t	243K
a-Si:H layer thickness	t_{Si}	50nm
Insulator thickness	t_{ox}	300nm
a-Si:H permittivity	ε_{Si}	1×10^{-10} F/m
Insulator permittivity	ε_{ox}	6×10^{-11} F/m
TFT flat-band voltage	V_{fb}	0.7V
Band mobility	μ_0	17 cm^2/Vs
Channel length	L	8μm
Channel width	W	80μm

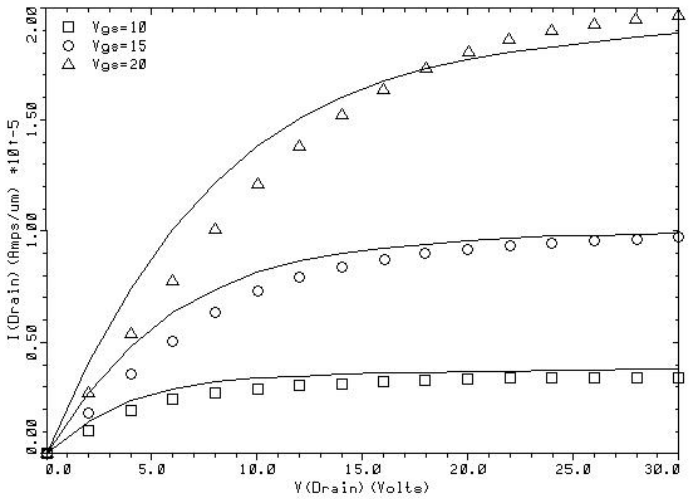

Fig.2 Measured (symbols) [26] and modeled (solid line) I_{ds} - V_{ds} data of a-Si:H TFT

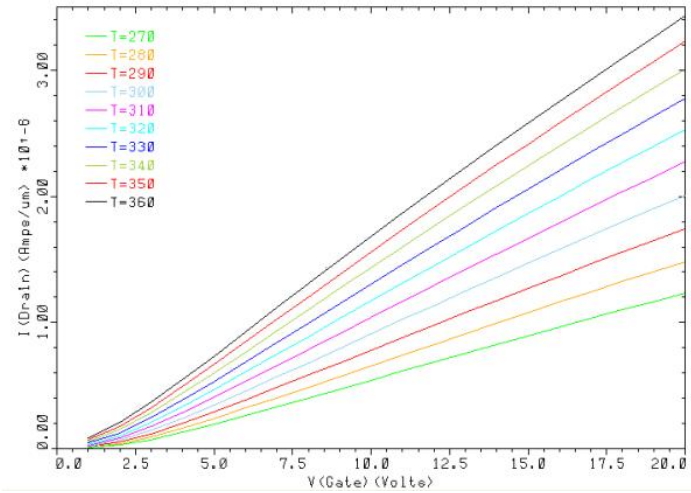

Fig.3 transfer characteristic curves of the a-Si:H TFT with V_{ds}=0.1V

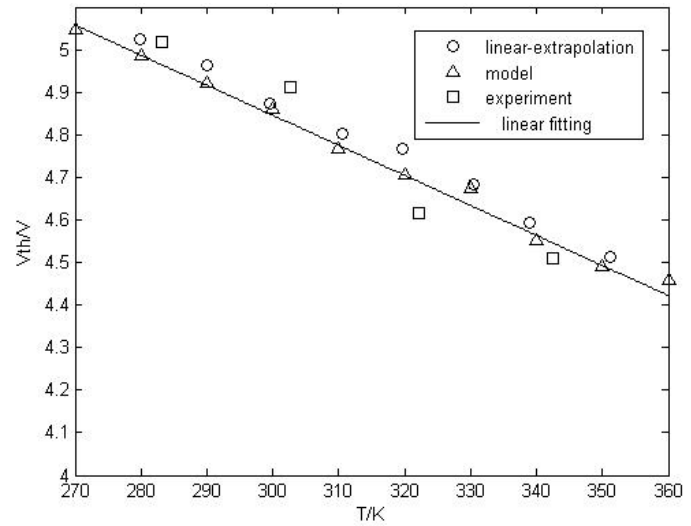

Fig.4 threshold voltage of the a-Si:H TFT with different extraction methods under different temperatures

4. Conclusion

Based on the temperature and the distribution of defect states, a extraction method of the threshold voltage for a-Si:H TFTs has been developed. In this model, it's unnecessary to extract the transconductance and it is analytical that easy to implement the circuit simulators. Results are favorably compared with the experiments available in the literature.

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References

[1] V. Ligatchev, Physica B-Condensed Matter, 337 (2003) 346-356.

[2] A. Nathan, G.R. Chaji, S.J. Ashtiani, Journal of Display Technology, 1 (2005) 267-277.

[3] J.T. Rahn, F. Lemmi, J.P. Lu, P. Mei, R.B. Apte, R.A. Street, R. Lujan, R.L. Weisfield, J.A. Heanue, Ieee Transactions on Nuclear Science, 46 (1999) 457-461.

[4] D. Flandre, V. Kilchytska, T. Rudenko, Ieee Electron Device Letters, 31 (2010) 930-932.

[5] S.W. Tsao, T.C. Chang, P.C. Yang, M.C. Wang, S.C. Chen, J. Lu, T.S. Chang, W.C. Kuo, W.C. Wu, Y. Shi, Solid-State Electronics, 54 (2010) 1632-1636.

[6] W.S. Lee, G.W. Neudeck, J. Choi, S. Luan, IEEE Transactions on Electron Devices, 38 (1991).

[7] Y. Liu, R.-H. Yao, W.-L. Deng, B. Li, Journal of Display Technology, 4 (2008) 180-187.

[8] M.L. Zhang, D.A. Drabold, European Physical Journal B, 77 (2010) 7-23.

[9] K.V. Ramesh, D.L. Sastry, Physica B-Condensed Matter, 387 (2007) 45-51.

[10] J.J. Hauser, G.A. Pasteur, A. Staudinger, Physical Review B (Condensed Matter), 24 (1981).

[11] S.C. Deane, R.B. Wehrspohn, M.J. Powell, Physical Review B, 58 (1998) 12625-12628.

[12] T.A. Abtew, M. Zhang, Y. Pan, D.A. Drabold, Journal of Non-Crystalline Solids, 354 (2008) 2909-2913.

[13] A.I. Yakimov, N.P. Stepina, A.V. Dvurechenskii, L.A. Scherbakova, Physica B, 205 (1995).

[14] M. Thamilselvan, K. Premnazeer, D. Mangalaraj, S.K. Narayandass, Physica B-Condensed Matter, 337 (2003) 404-412.

[15] J. Li, D.A. Drabold, Physical Review B, 68 (2003).

[16] K. Murayama, Physica Status Solidi C, 8 (2011).

[17] R. Schwarz, Journal of Non-Crystalline Solids, 227 (1998) 148-152.

[18] K. Hattori, T. Hirao, Y. Musa, H. Okamoto, Physical Review B (Condensed Matter and Materials Physics), 64 (2001).

[19] T. Rudenko, V. Kilchytska, M.K.M. Arshad, J.P. Raskin, A. Nazarov, D. Flandre, 2011 12th International Conference on Ultimate Integration on Silicon (ULIS 2011), (2011).

[20] M.S. Shur, H.C. Slade, T. Ytterdal, L. Wang, Z. Xu, M. Hack, K. Aflatooni, Y. Byun, Y. Chen, M. Froggatt, A. Krishnan, P. Mei, H. Meiling, B.H. Min, A. Nathan, S. Sherman, M. Stewart, S. Theiss, Amorphous and Microcrystalline Silicon Technology - 1997 Symposium, (1997).

[21] G.E. Possin, Amorphous Silicon Technology - 1991 Symposium, (1991).

[22] A.K. Kapoor, S.C. Jain, J. Poortmans, V. Kumar, R. Mertens, Journal of Applied Physics, 92 (2002) 3835-3838.

[23] T.A. Abtew, M. Zhang, D.A. Drabold, Physical Review B, 76 (2007).

[24] S. Marianer, B.I. Shklovskii, Physical Review B (Condensed Matter), 46 (1992).

[25] M. Shur, M. Hack, Journal of Applied Physics, 55 (1984).

[26] M. Shur, M. Hack, J.G. Shaw, Journal of Applied Physics, 66 (1989) 3371-33803380.

[27] R. Bruggemann, Thin Solid Films, 427 (2003) 355-357.

[28] M. Hack, R.A. Street, Applied Physics Letters, 53 (1988) 1083-10851085.

[29] J. Kakalios, R.A. Street, Physical Review B (Condensed Matter), 34 (1986).

[30] R.A. Street, IEEE Transactions on Electron Devices, 36 (1989).

[31] A. Kuo, T.K. Won, J. Kanicki, IEEE Transactions on Electron Devices, 55 (2008) 1621-1629.