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Preparation and processing of big data during of industrial testing of VLSI

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Abstract

The integration level of modern VLSI allows developers to place an entire digital device on a chip (System-от-Chip technology), which dramatically increases the amount of data on testing such VLSI. The most alarming situation is observed when testing VLSI memory, which is both an independent VLSI and one of the main blocks of a digital system. The process of their production includes up to 1000 technological and control operations, for which it is necessary to memorize hundreds of parameters. As a result, testing the memory required for practice by modern VLSI methods may take several years. The article proposes a hardware and software complex for industrial testing of VLSI, in which the developer is excluded from the two-way chain «algorithm of testing ↔ topology», which made it possible to effectively implement the mechanism for localizing of the topology errors by directly linking them with test vectors. The client-server system of the «*Sigma Viewer*» complex and the «*Lorenz*» data analysis environment are described, which, using the new original «*RSTL*» data format, provide storage and processing of an almost unlimited amount of

interoperational exchange metadata. The complex operating on the basis of the «STeeL» language, capable of processing hundreds of thousands of test vectors in real time.

Keywords: industrial testing of VLSI, big data on testing of VLSI, software, hidden defects of integral structures.

Introduction

A necessary condition for building an effective system of traceability of objects of labor in production is the preservation of all, without exception, the results of measurements of a large mass of parameters at all productional operations of testing and manufacturing of VLSI. The matter aggravates increasing complexity of configuring test equip-ment and the increasing complexity of VLSI climate tests [1, 2, 3].

When trying to solve this problem, engineers are faced with the problem of storing and processing big data, the volume of which can reach tens of gigabytes, and if it is necessary to perform interoperative data analysis - several terabytes.

The subject of labor in the general cycle of technological preparation of VLSI production in this article means the completed result of a separate production operation of the specified cycle. Moving from one operation to another, one object of labor (for example, a wafer) is transformed by cutting operations into another object of labor - crystals, which at the stage of packaging form a new object of labor - microcircuits. Traceability of objects of labor is usually understood to mean the preservation of the entire history of manufacturing the VLSI , for which the test results from all, without exception, its manufacturing operations remain available for analysis up to the finished microcircuit is received.

If all interoperational connections will be preserved in the process of transforming one object of labor into another, it will be possible to define scientifically based production test standards, which will dramatically reduce the number of defective crystals on the wafer. However, at present, due to the information gap between individual operations, the possibility of conducting an effective interoperative analysis is completely excluded..

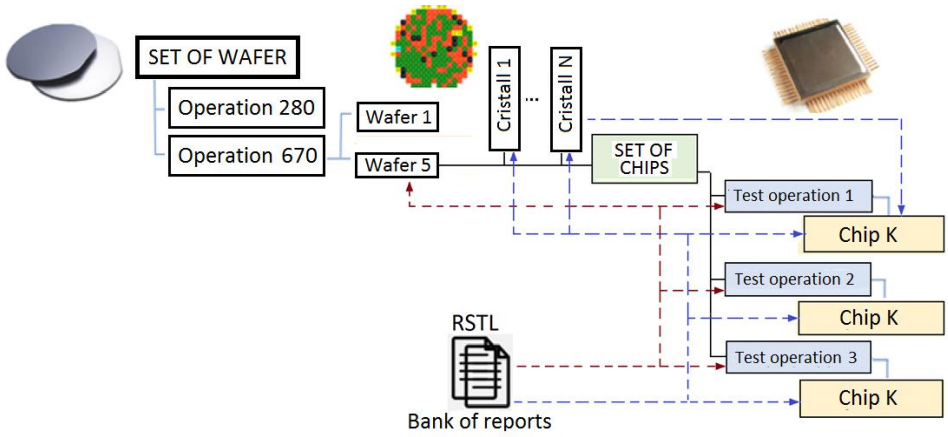

Figure 1. The process of indexing reports and linking report data to objects of labor, operations and batches of products

An additional factor aggravating the situation is that equipment from different manufacturers on the market stores test results in formats that do not provide saving of service and debug information, without which it is generally impossible to conduct an interoperative analysis of failures.

Suggested method

That task is solved using the "Functional Test Studio" software and hardware complex, developed by the authors on the basis of the VLSI testing route [4], which raises the process of preparing and conducting industrial tests of VLSI to qualitatively new automation level since it implements a mechanism for localizing errors in the VLSI topology, directly linking the places of their detection with test vectors. The complex operates on the basis of the high-level cross-platform programming language STeeL, which implements a close relationship of mathematical and topological VLSI model according to the block diagram shown in Figure 2..

The theoretical basis for the functioning of the complex is a multi-stage two-way mapping of a set of input actions X (test tables, primitive cubes, etc.) onto a set of test objects Y, introduced using the functions f_1 and f_2, which can be represented as:

$$\begin{cases} f_1 \Longleftrightarrow f_2 \\ f_1 : X \Rightarrow Y \\ f_2 : Y \Rightarrow X \end{cases} \qquad (1)$$

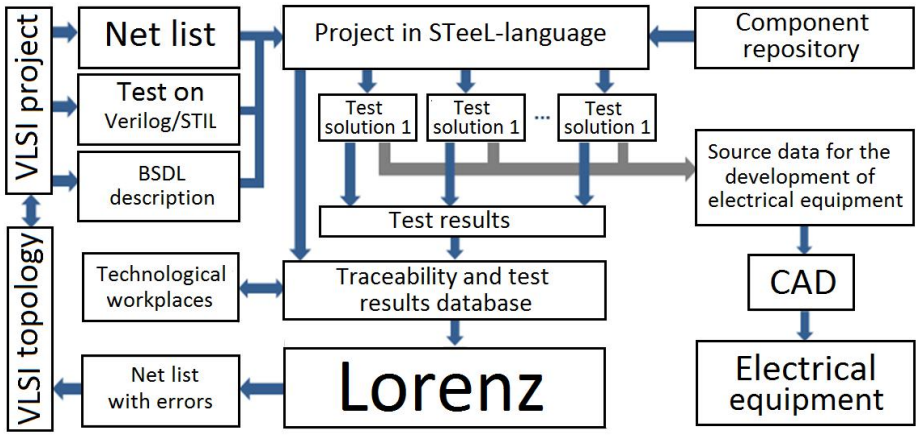

Figure 2. Block diagram of the hardware-software complex of testing VLSI

Here, as input influences, test vectors are used, given by binary {0, 1}, ternary {0, 1, *z*} and polysemantic alphabets, as the most using in the practice of using equipment for functional testing of VLSI. One of the examples of mapping (1) is a two-way connection of a set of elements of test vectors with a set of gates in a topological VLSI model, implemented by the expressions:

$$\begin{cases}(f_1^1 : V \Rightarrow P_i) \rightarrow (f_1^2 : P \Rightarrow D_i) \rightarrow (f_1^3 : D \Rightarrow T_i) \rightarrow (f_1^4 : T \Rightarrow B_i) \\ (f_2^1 : B \Rightarrow T_i) \rightarrow (f_2^2 : T \Rightarrow D_i) \rightarrow (f_2^3 : D \Rightarrow P_i) \rightarrow (f_2^4 : P \Rightarrow V_i)\end{cases} \qquad (2)$$

where: *V, P, D, T* and *B* represent, respectively, sets: the elements of the test vector $\{V\}$, the register $\{P_i \in P\}$, to which the vector element refers, the flip-flop $\{D_i \in D\}$, to which the register P_i refers, the transistor $\{T_i \in T\}$, which is referenced by the flip-flop D_i, and the gate $\{B_i \in B\}$, which is referenced by the transistor T_i. Graphically, correspondences (2) are presented in Figure 3.

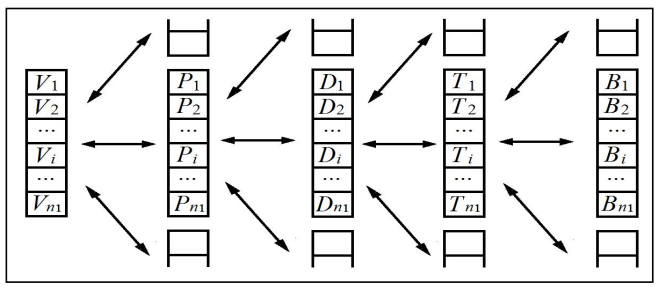

Figure 3. Multi-stage two-way communication: "test ↔ topology"

Technically formulated correspondences are implemented when testing digital VLSI using JTAG interfaces and are continuously supported at all operations of the technological process of VLSI functional control without exception, including a testing of the contact devices [5].

For example, when testing VLSI in production conditions when moving along the upper branch of communication (2):

$$(f_1^1 : O_1 \Rightarrow O_{2i}) \xrightarrow{f+} (f_1^2 : O_2 \Rightarrow O_{3i}) \xrightarrow{f+} \ldots \xrightarrow{f+} (f_1^{n-1} : O_{n-1} \Rightarrow O_{ni}) \qquad (3)$$

all information received about the testing progress is storing in the database, and when analyzing the test results (lower communication branch), it is used to localize failures at the level of a batch of wafers O_1, a batch of crystals O_2, a batch of microcircuits O_3. At the same time, additional transformations ($f+$) between the levels perform the detailing of the stored information, differentiating it by types of test control, types of accompanying documents, types of personnel involved, and so on. Similar chains of two-way communications are implemented in the system as well at other stages of the VLSI technological preparation, in particular, onto stage ensure the software cross-platform.

Thus, full coordination of all blocks of the structural diagram of that complex is ensured without loss of data conversion information during inter-block transmission. In the testing algorithm using the tools of the system language STeeL, test parameters are set, including test separation attributes, attributes of creating and using a relay switching scheme, attributes of mirroring controlled signals for tests of all types. When the next input test arrives, it is automatically transformed into test suites, and the STeeL compiler preserves the correspondence of the original test lines or SCAN labels to the data in the output files. This information is used to localize errors in the topology using error maps received from production equipment.

The complex also provides the ability to develop tests at once for the entire fleet of equipment available at the enterprise with the preservation of all the necessary information for post-test analysis on the operations of parametric, visual and functional control of plates and microcircuits. At the same time, on each of the 900 technological operations of testing VLSI there are automatically saved hundreds of parameters of various types required for the subsequent analysis of metadata.

In these conditions, technologies for collecting and processing data on all stages of VLSI production are becoming more and more in demand. Eg, only the most important data that need to be saved on test control operations with reference to a specific subject of labor are:

– logs of testing;

– multidimensional tables of functional control results;

– tables with the results of parametric control;

– logs of loading functional Real-time tests for microprocessors;

– maps of errors of passing functional tests;

– data from sensors of equipment operation;

– data on temperature profiles;

– graphic images.

The amount of data of each of the listed types for each batch of wafers is measured in tens of gigabytes, since it contains the results of measurements of hundreds of different types of parameters wich are obtaining during the production testing of VLSI. Moreover, the amount of data to need stored and processed at the stages of interoperational analysis is already measured by terabytes. In these conditions, very stringent requirements for *scalability*, fault tolerance, and locality are imposed on the existing data presentation formats.

By scalability, we mean the ability to add new types of test results, objects of labor and new technological operations to the technological route of testing VLSI. The requirement for resiliency of formats concerns data processing methods that must provide resiliency both during storage and during data processing. The requirement for data locality is due to the fact that VLSI production includes dozens of pieces of equipment, some of which provide storage of results only on equipment, i.e. some of the data is distributed across a large number of workstations. In order to reduce the cost of constant data transfer between the processed system and data storage locations, it is necessary to ensure the collection and centralized storage of data from all equipment. To ensure the principle of data locality, the data processing system must be located on the same computer system as all data.

At the same time, none of the known data presentation formats is able to satisfy all the listed requirements. For example, the format GDF (Generic Data Format) is a good choice for short test programs with few controllable parameters only. The format STD (Standard Test Data) does not allow storing multidimensional data structures as a set of curves, tables and bit matrices, as well as links to data diagnostics results (photographs of the state of the needles of contact probes, curves describing the thermal profile during the test, etc.). The format XML also cannot be applied due to its great redundancy. A common drawback of the XML and GDF formats is the container principle of storing data with their help, which increases

the processing time of the file and does not allow receiving data from files, the recording to which was interrupted due to a hardware failure.

The RSTL format, proposing in this article, is free from the above drawbacks. The format uses a cross-platform approach to VLSI testing, in which all interoperational communications on subjects of labor and test results are stored in the results bank in accordance with their constructive hierarchy. Additionally, the names of test programs for each operation, used sets of test vectors and their versions, as well as connections of test vectors with a set of gates in the VLSI topological model, implemented by expressions (2), are saved.

Processing of test results

Ensuring the traceability of objects of labor implies uniform access to the measurement results for employees of various departments of the enterprise participating in the analysis of data and is one of the urgent tasks in modern production conditions. To solve such a problem, it is required to automate the measurement process at control operations and provide the ability to quickly process data from several operations or between batches. Traditionally, this problem is solved by the software modules LabView and Agilent VEE, however, the inclusion of a third-party application into these moduls significantly complicates each that module.

To solve this problem, within the framework of the *FT Studio* complex, the client-server system *Sigma Viewer* and the built-in data analysis environment Lorenz were developed, which use the RSTL format for storing the results and allow, among others, to solve the next tasks:

– collection of measurement results from various measuring equipment, taking into account accompanying information;

– display of measurement results in a uniform interface;

– analysis of measurement results using the built-in Python language [6] and support for SQL queries;

– preparation of reports on the measurements performed using templates.

The functional diagram of the information infrastructure of the "Sigma Viewer" system, shown in Figure 4, has a single interface for interaction with client programs, which ensures

the interaction of personnel with measuring and test equipment. The system infrastructure allows accumulating complete statistics on all measured parameters of microcircuits and semiconductor wafers and analyzing them in order to identify the causes of VLSI failures. In addition to the main ones, the system provides administrative functions that allow you to enter the differentiation of the rights of employees to perform various operations.

The system consists of server and client parts. *The server part* is controlled by the original DBMS, solving the problems of collecting and indexing measurement results, organizing an interface with the client part and storing in the database information about objects of the subject of labor, configurations of measuring equipment and ets. *The client part* consists of client programs for equipment control, programs for analyzing results and a system for developing functional tests. Client-side applications have a wide range of tools for data analysis, allowing, for example, to analyze the distribution of a given parameter over a plate with the output of the results in the form of graphic and text forms.

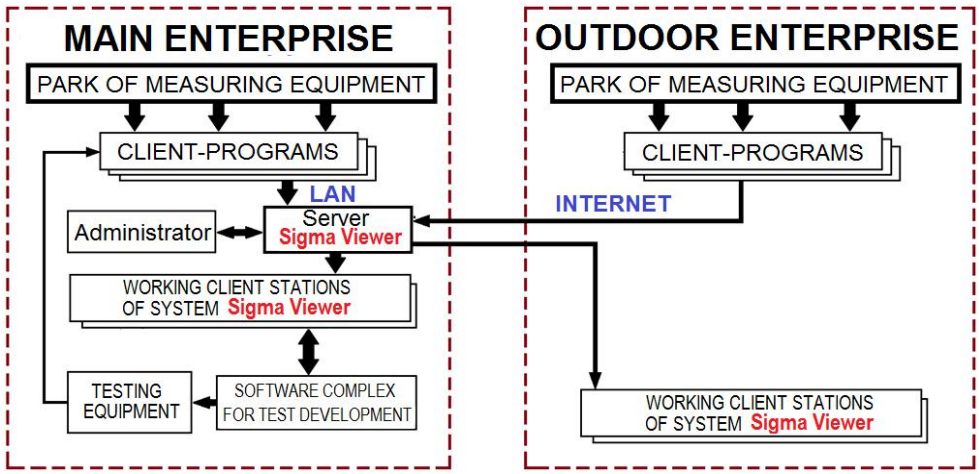

Figure 4. Functional diagram of the «Sigma Viewer» system

RSTL format unlike the knowns :

– allows multiple inheritance in tests, which allows you to automate the process of generating reports;

– allows you to store an unlimited amount of metadata, including hierarchical, with the ability to link to a specific report, subjects of labor or the result of analysis;

– contains tools for storing the pseudocode of the testing algorithm directly in the report to ensure guaranteed rechecking of the object of work, for example, in case of a complaint several years after the release of the chip;

– uses an ignore level code that allows you to exclude commands below the level indicated

by this code, which significantly reduces the analysis time.

In addition, the RSTL format supports the description of the relationship between the test and a specific crystal in the chip, which allows, after the completion of the interoperational analysis, to obtain the production history of the crystal installed in a specific chip, according to the diagram shown in Figure 5.

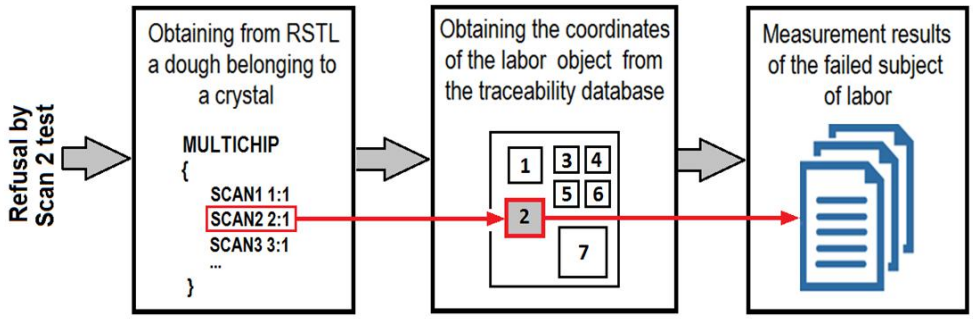

Figure 5. Obtaining the history of chip production

Cross-operational data analysis and visualization of results

The ability to simultaneously access the measurement results of various operations allows for cross-operational data analysis. For example, it is possible to carry out a correlation analysis of the results of electrical measurements and functional control of a semiconductor wafer in accordance with its results of electrophysical measurements at different stages of crystal production. As the objects of labor pass along the technological route, the connections between them remain in the system. For example, the unique serial number of the microcircuit traces the entire route of its manufacture and the collection of all monitored parameters in the process of manufacturing the microcircuit. This approach multiplies the efficiency of preparing production tests, allowing the developer:

– describe tests not in the form of a test table, but as parameterized algorithm in the STeeL language [7], wherein during the compilation of the algorithm, a unique for each crystal test is dynamically built;

– to implement dynamic generation of a test table when starting a test according to conditions depending on the results obtained in previous operations, which allows instead of a complete test to launch of the minimum necessary one;

– to analyze only faulty crystals for specified areas of cells and present the results in the form of graphic cards of validity.

Currently, factories mark defective crystals with paint, which practically excludes the possibility of a serious statistical analysis of the test results of wafers. This article offers an electronic map showing the level of crystal defects on a wafer (defect map). For example, in the case of memory microcircuits testing, the entire wafer is divided into crystals shown by squares in Figure 6. Each square die contains 16 memory banks.

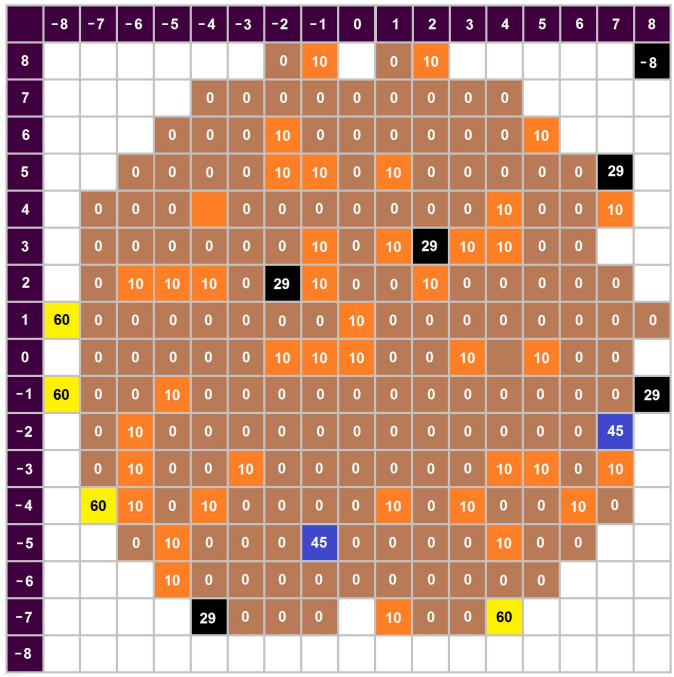

Figure 6. The validity card of the wafer and the contents of one of its crystals

In this case, the state of the memory banks is displayed on the defect map, identified by the corresponding defect code. Banks located in the center of the plate, due to technological features, can work a little faster than edge banks, or have other supply voltage ranges. For example, by denoting the number of working banks on one die with the symbol K, you can display the K numbers in the cell of each crystal using the entered the defect maps. The latter in this case receive the status of the map of the distribution of parameters over the plate. For clarity, each "crystal cell" has highlighting of a specific color: from green (no errors) to red (maximum number of errors). So, Figure 7 on the left shows in which areas of the wafer the crystals with the maximum K number are located. The same figure in the center and on the right shows how this pattern changes for each crystal when the supply voltage and test frequency [8] change accordingly.

Figure 7. Distribution cards by the wafer of the number of working banks

Brief conclusions

1. Methods for collecting, storing and analyzing big data for industrial testing of modern VLSI with their reference to specific objects of labor (plates, crystals, chips, etc.) are proposed.

2. A universal format for storing big data (RSTL) for the results of test, parametric and interoperational control of VLSI is proposed. The format, unlike the known ones, is resistant to failures of test equipment and is able to maintain the storage of complete information along the entire VLSI design route, measured at the stage of correlation analysis by units of terabytes.

3. The functional capabilities of the "Functional Test Studio" hardware and software complex are described, which for the first time allows for the interoperational analysis of large data of VLSI production testing in automatic mode.

4. Within the framework of the complex, an automatic system of interoperational analysis "Lorenz" with support for the Python language and well-known libraries for processing big data, adapted for the analysis of results in the production of VLSI, is implemented.

5. Demonstrated tools for visualization of big data for all types of VLSI failures on the technological route of its production. These tools use a direct connection of the locations of localization of topology errors with test vectors.

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